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HYBRID TECHNOLOGY COST REDUCTION AND RELIABILITY IMPROVEMENT ST--ETC(U)
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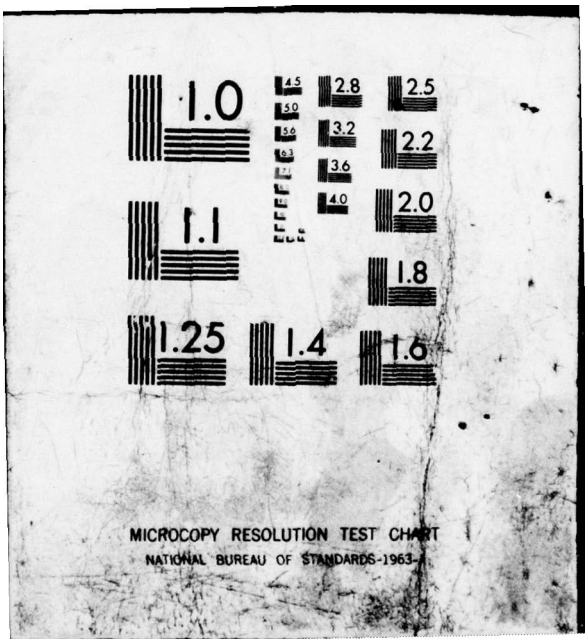
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(8) A high cost element in the production and deliver
volume military hybrid is qualification per MIL-M
prime reason is the large number of qualification
in some cases exceeding the planned production ru
handled this problem in the past?

Responses: 10

1) Waivers, qualification by similarity.
2) Not qualified the parts.
3) Use of tighter in-process controls and screen
4) Use of limited quantity procurement provision
paying the cost.

What changes would you propose in MIL-M-38510 to r
of hybrid qualification?

Responses: 10

1) Qualify the line and the process periodically.
2) Qualify by similarity, and qualify function fo
performance.
3) Add more stringent process controls.
4) Qualify totally dependent on individual procur
5) Delete all tests, and add electrical tests at
6) Intelligent enforcement of the requirements.

(9) Have the hybrid microcircuits reached the complexi
systems and should they be controlled as subsystem
qualification rather than treated as components?

Responses: 9

Yes: 9 No: 0

The large number of screening requirements on a hybrid may be due to the complexity of the technology. The hybrid industry employs an expanding number of materials and processes which are independent or may interact with previous and following operations in the fabrication flow. This may result in additional material problems resulting in a new screen to control new potential material failure combinations.

One solution to this problem may be the certification of each hybrid manufacturing line based on their particular processes. A set of test structures then could be used to insure continued line certification and a reduction of in-line screening costs. After certification each hybrid type would then be qualified per program requirements.

(10) Do you feel that a military developed line certification program would assist the industry in reducing hybrid costs without degrading product reliability?

Responses: 13

Yes: 8 No: 5

Comments:

1) The military would specify additional controls on operators.
2) (Yes) There would be an elimination of duplication.
3) If the same processes and components were used, then the line certification method is the same.
4) Materials and technology change too fast.

(11) Should the military control hybrid design rules such as:

- Minimum design requirements (line widths, power levels, laser trim limits, etc)?

(11) (Continued)

- Allowable and disallowable materials and techniques?
- Methods of process control and screening?
- Requirements for qualification?

Responses: 14

Yes: 3 No: 11

Comments:

1) Military control would demand outmoded processes due to new technology.
2) Manufacturers should maintain minimum standards.
3) Costs.
4) Quality in workmanship - customer gets what he wants.

(12) Should the military standardize on <u>one</u> set of hybrid processes controlled through a military specification? Potential advantages are lower costs, increased reliability, easy second sourcing and repair.

Responses: 13

Yes: 1 No: 12

Comments:

1) (No) This would limit new process development.
2) Would force some houses out of business.
3) Hybrids are a system problems and processes vary.

(13) What would you consider to be the disadvantages and advantages of a standardized industry hybrid process?

Responses: 11

(13) (Continued)

Advantages

1) None.

2) Uniformity in materials, equipment, and training.

3) Easier government approval.

4) Increased small business participation.

Disadvantages

1) Stagnation - old technology.

2) Extra costs for retooling.

3) Decreased performance.

4) Fewer participating companies.

(14) Recent military system requirements have specified packaging methods that will allow the military user to return the failed hybrid to a depot and repair it as necessary to recover the use of expensive hybrids and reduce spares. What type of support must the industry supply the military customer to allow the above to be successful? (Repair techniques and processes, test software, test hardware, etc.)

Responses: 11

1) Let the major subcontracts to industry.

2) Supply processes and procedures.

3) Supply instructions.

4) Experience or training.

(15) If the military performs the repairs, what impact will that have on the manufacturers product warranty?

Responses: 11

1) Warranty would be void (unanimous).

(16) Will repairs by the customer be a viable solution to reducing system life-cycle costs?

Responses: 12

Yes: 4 No: 8

Comments:

1) Customer will not have personnel and organization competent enough to do the work.

2) (Yes) Due to experience and knowledge gained in repair and troubleshooting techniques.

5.0 HYBRID MICROELECTRONIC FAILURE MODES

The general discussion of hybrid microelectronic yield problems from initial design through processing to actual application can be subdivided by looking at known failure modes of hybrids during (1) Manufacture (In-Process Rework) and (2) Application (Field Failures).

Manufacture - The fabrication of hybrid microelectronics from substrate through final acceptance test normally requires a certain amount of in-process rework. The amount of this rework directly affects the hybrid assembly costs and yield and has a direct influence on the final product cost and reliability.

(1) Past industry studies have indicated that the most significant in-process failures modes are related to active devices and wire bonds. What is the percentage of failures you encounter that require in-process rework.

Responses: 11

	0-5%	6-10%	11-25%	26-45%	46-65%	66-85%	86-100
Active devices	0	2	2	3	1	2	1
Passive devices	7	2	2	0	0	0	0
Wire bonds	3	4	2	2	0	0	0
Substrate shorts/opens	9	1	1	0	0	0	0
Other	5	2	3	1	0	0	0

(2) What IR&D efforts are you scheduling or have you implemented to reduce these rework percentages?

Responses: 11

(2) (Continued)

1) Process and materials bonding controls.

2) Better screens.

3) Incoming testing of chips.

4) More die tests.

5) None.

6) Increase training.

7) Use of hermetic chip carriers.

8) Investigate tape bonding.

9) Controls on organics.

10) Develop universal probing fixtures.

(3) What government/industry efforts will be required in the 1980's such as new processes, tape bonding, and die pretesting to reduce these rework costs?

Responses: 10

1) Pretesting, rework with diagnostics.

2) Testing over temperature range.

3) Make available test programs and low cost chip testers.

4) Guarantee die shipments that work.

5) Develop tape bonding for industry acceptance.

6) Develop better wire bonding screens.

7) Newer procuring and specifying processes.

8) Develop hermetically sealed, pretested dice.

(4) Consider a hybrid that is reworked a finite number of times and passes all visual and in-process screens and tests versus one that passes the same tests but never sees rework....how would you compare their equivalent long term reliability?

(4) (Continued)

Responses: 13

Same 7

Reworked Part Lower 6

Comments:

1) Rework handling may cause failures.

2) Rework causes additional heat cycles.

3) Put bonds on new sites.

4) Good QC practices produce fair rework.

5) Reliability is the same as shown by field experience.

(5) Should MIL-M-38510 allow infinite rework if the hybrid continues to pass all MIL-STD-883 screens?

Responses: 13

Yes: 6

No: 7

(6) Should MIL-M-38510 rework limits be:

Responses: 13

tightened? 2 Degree: a small amount

relaxed? 11 Degree: a medium-small amount

Application - Field failures can be separated into two areas, low power and high power hybrids. Past industry studies still indicate the prime failure modes occurring during manufacture are due to active devices, but other items such as contamination become more dominant once the product is in the field.

(7) In your analysis of field failures, where have you encountered your major field return problems?

Responses: 6

	Low Power %	High Power %
Active devices	(5) 36%	(3) 25%
Wire bonds	(6) 13%	(2) 10%
Contamination (Chemical)	(6) 18%	(3) 16%
Loose particles	(5) 10%	(1) 0%
Package seal	(5) 11%	(2) 8%
Device attachment	(5) 6%	(2) 30%
Solder joints	(5) 10%	(2) 50%
Passives	(5) 4%	(3) 20%
Other	(5) 28%	(3) 25%

(8) What methods do you employ to control in-process loose particle contamination problems? Effectiveness?

Responses: 11

1) PIND
2) Precap visual; excellent result, unknown results
3) Blow, wash, and visual inspection
4) Laminar flow at preseal
5) Evaluation by recovery and identification of poor processes - very effective

(9) Do these controls vary based on the quality level of the part to be delivered?

Responses: 11

Yes: 4 No: 8

(9) (Continued)

Comments:

1) Cost effectiveness - prime factor

2) Different customer requirements

(10) Particle contamination controls being currently employed by the industry include a range of methods such as a simple wash to PIND testing and Parylene Coatings. Which do you employ?

Responses: 11

Wash	9
PIND	4
Parylene	1
Visual Airblast	1
Visual Laminar Flow Inspection	1

(11) Which of the above methods do you feel will become the prime method of particle control during the 1980's?

Repsonses: 12

Wash	3
PIND	4
Parylene	2
Visual	2
Others	2
No Problem	1

(12) What research is still required to insure that product costs and long term reliability are not adversely effected by employment of these loose particle control methods?

(12) (Continued)

Responses: 10

1) Historical Analysis
2) Better Conformal Coatings
3) Proper Seal Techniques
4) None
5) Redundant System Design
6) Removable Coatings Similar to Parylene

(13) What process research is required to reduce the cause of other field application failure modes?

Responses: 8

1) Seals and coatings.
2) More automation in production-process control.
3) Better understanding of failure causes.
4) Time and temperature studies..
5) Improved passivation at chip level.

(14) What has your experience been with moisture related problems in hybrids?

Responses: 10

1) Very small problems.
2) At sufficient water content, moisture will kill a hybrid.
3) Poor seals.
4) Ionic contamination.
5) Performance degradation.
6) Corrosion of wire bonds (in non-hermetic seals).

Some industry reliability papers have identified spittle residue, which occurs during hybrid processing, as the cause of several hybrid failure modes. These include gold migration, disappearing aluminum, and silver migration.

(15) Have you encountered any known hybrid reliability problems due to spittle?

Responses: 11

Yes: 4 No: 7

(16) Do you employ in-process controls to eliminate spittle contaminatio

Responses: 11

Yes: 4 No: 7

6.0 HYBRID DESIGN

The high cost and low reliability of hybrids in system designs, in some applications, may be due to the methods typically used in incorporating an electronic design into a hybrid package. Hybrids in many cases are the last resort when other packaging concepts do not meet the needs of the program. This may result in a hybrid that is unique in design, pushing design limits, raising costs and affecting final product reliability.

The following questions are designed to identify the extent of these problems and ways that the industry can ensure that hybrid design is a part of the total integration of microelectronics and electronic packaging.

(1) Hybrid designers can be given either a black box specification (Form,Fit, and Function) or a circuit schematic that must be reduced one-for-one to a hybrid design. What percentage of your designs are:

Responses: 12

	0-10%	11-20%	21-40%	41-60¢	61-80%	81-100%
Black Box	7	3	0	1	1	0
Schematic	0	1	0	1	1	9

(2) At what level are/should your hybrid designers to involved in the conceptual design stage to maximize the effectiveness of hybrid designs (% of time)?

Responses: 9

1977

	0-10%	11-20%	21-40%	41-60%	61-80%	81-100%
RFQ	4	0	3	0	0	0
El Funct. Blk Diag	5	2	1	0	0	0
Pkg Concept Form	2	1	3	1	0	1
Pkg Partitioning	1	1	3	1	0	2
Other	0	1	2	0	0	0

1978

	0-10%	11-20%	21-40%	41-60%	61- 80%	81-100%
RFQ	4	2	2	0	0	0
El Funct. Blk Diag	3	4	1	0	0	0
Pkg Concept Form	2	2	2	0	0	2
Pkg. Partitioning	1	3	2	0	0	2
Other	0	2	1	0	0	1

(3) Can an electronic circuit schematic be reduced one-for-one and retain the advantages of hybridization?

Responses: 11

Yes: 4 No: 6

Comments:

1) (No) Difficult to achieve component values and tolerances
2) (yes) Higher density can be achieved
3) Thermal considerations
4) Concern of costs, parts, and processes.

(4) When designs are reduced 1/1, what percentage of the time are the specified individual components compatible with your prime hybrid processes?

Responses: 11

0-15%	16-35%	36-55%	56-80%	81-100%
0	1	1	2	7

(5) How often do you encounter chip procurement problems of specified devices in 1/1 designs?

Responses: 10

0-5%	6-15%	16-35%	36-55%	56-80%	81-100%
1	4	3	2	1	0

(6) Do your designers employ a Preferred Parts List (PPL)?

Responses: 12

Yes: 6 No: 6

(7) If so, what is the cost impact on parts procurement?

Responses: 6

Reduction: (3) a small amount

Same: (2)

Increase: (1) a small amount

(8) When newly released semiconductor devices are used, how often do you encounter problems with process compatibility?

Responses: 11

0-5%	6-15%	16-35%	36-55%	56-80%	81-100%
4	2	2	2	1	0

Comments:

1) Poor process controls
2) Inadequate specification sheet
3) Bonding pad sizes
4) Difficulty in procuring chips
5) Backing metalization.

(9) When a hybrid design is being finalized, do you employ a Preliminary Design Review, Critical Design Review with:

Responses: 11

customer? Yes 7 No 1

internally? Yes 11 No 0

(10) Do you perform a formal thermal analysis on your hybrid designs?

Responses: 12

Yes 8 No 4

Level

1) Functional (2)
2) Breadboard (2)
3) Depends upon time and money (1)
4) High (1)
5) Only on request (1)

(12) Do you perform a reliability analysis on the proposed hybrid design?

Responses: 11

Yes: 5 No: 6

Method:

1) Method 217 as required (3)
2) As required in 750
3) RADC handbook

(13) What are your present design limits in the following areas?

Responses: 11

I/O Pin Count	40-50	60-65	70	120	200-280	None
1977	3	1	3	1	0	1
1987	0	0	4	0	3	1

Substrate Size (in^2)	1-2	3-4	5-6	8-12	16-18	20-30	None
1977	2	3	2	0	2	0	1
1987	0	3	0	2	2	1	1

Thermal Density (W/in^2)	2-6	10	15	25	50	100	200
1977	5	1	2	1		1	1
1987	3	0	1		1	1	1

Chip Count	10-25	30-40	50	80	100-200	140	None
1977	3	1	3	1	2	0	1
1987	0	2	2	0	1	1	1

Wire Bonds	200-300	400-700	1000-2000	5000	None
1977	4	2	4	0	1
1987	0	2	3	1	1

Density (Dev/in^2)	7	10-15	16-30	35-40	Npne
1977	1	4	0	3	1
1987	1	3	0	0	1

(17) To what extent do your designers employ Computer Aided Design (CAD) tools in completing a hybrid design?

Responses: 12

1) Only in critical design layouts (3)
2) Less than 10% (2)
3) 0 (2)
4) Minimum (2)
5) Extensively, most everywhere (2)
6) As much as possible

(18) Do you intend to increase the number of engineering CAD aides in the next ten years?

Responses: 10

Yes: 9 No: 1

Comments:

1) Substrate layout using CAD design will increase (3).
2) Complete device modeling (2)
3) Yes for multilayer circuits
4) Electrical circuit analysis

7.0 THICK AND THIN FILM SUBSTRATES

(1) Does your facility make both thin and thick film circuits?

Responses: 11

Yes	No
8	3

% of each

Thick Film: Responses: 10

40	45	80	85	
1	1	5	3	

Thin Film: Responses: 8

0-5	5-10	10-15	40	60	
2	2	2	1	1	

(2) What is your opinion on the trend of thick versus thin film circuits? Why!

Responses: 11

a) Thick film will predominate due to lower processing costs. 11

b) Thin film serves where high resolution or precision and stability is demanded. 3

c) Thick film is less fragile. 2

(3) What percentage of your hybrid circuits will be thin and thick in 1987?

Thick Film

Responses: 10

50	90-95	95-100
1	4	5

Thin Film

Responses: 6

5	10	50
1	4	1

(4) Do you laser trim your film resistors?

Thick Film

Responses: 11

Yes	No
9	2

Thin Film

Responses: 6

Yes	No
5	1

% of each

Thick Film

Responses: 6

20%	80-90%	90-100%
1	2	3

Thin Film

Responses: 3

80-90%	90-100%
1	2

(5) Do you feel that there are cost/reliability advantages of one film type over another? Why?

Responses: 10

a). Cost: Thick film, Reliability: Thin Film 8

b) Equally Reliable 3

c) Use Thick Film everywhere but microwave circuits 1

d) More consistent, stable, temperature effects - Thin Film - 1

Thin Film Circuits

(1) What percentage of your thin film applications are on:

Silicon

Responses: 8

0-5	10	50	60
4	1	2	1

Ceramic

Responses: 9

40	60	80	90	95-100
1	1	2	1	4

Type

Responses: 6

a) 99.6 2

b) Microwave Circuits 1

c) 99% Alumina 2

d) Nicrome and Chrome silicon 1

(2) Which methods of processing do you use?

Responses: 9

evaporation/sputter/masks 5

chemical etch 8

procurement 3

(3) What are the current processing limits, typical designs, and goals in the following?

Responses: 7

a. Conductive Layers

	1	2	3	4	5
max	4	2		1	
typical	6	1			
1987 Goal	2	1	1		1

b. Resistors valve Responses: 2

	<50 K	1MΩ	10MΩ
max		1	1
typical	2		

TC Responses: 3

	100PPM	50PPM	75PPM
max	1	2	
typical		2	
1987 goal			1

Tolerance — Responses: 4

	±¼ %	± 1%	± 2%	± .01%	±5-10%
max	1	1			
typical		2	1		1
1987 goal				1	

c) Substrate Area (Inches) — Responses: 5

	2x2	1x1	3x2	3x4	5x5	5x6	
max	2		1	1	1		
typical	2	1	1				
1987 goal				1		1	

d) Conductor Lines/Spaces (Mils)

Responses: 5

	4/2	2/2	5/5	3/3	10/10
min		2	1	1	
typical	1	1	2		1
1987 goal	1				

(4) Type of film materials

Responses: 9

a) Gold - Nichrome 8

b) Chrome 1

c) Copper 1

d) Propriatory 1

(5) What is your substrate processing yield?

Responses: 7

a) 5-25% _____

b) 25-45% _____

c) 45-65% 2

d) 65-85% 4

e) 85-100% 1

(6) What is your high cost element in thin film processing?

Responses: 3

	30%	50%	60%
a. Deposition	1	1	1
b. Etching		1	2
c. Photo-resist	1		

(7) Where are your IR&D efforts being spent in the next 10 years to improve thin film hybrid reliability and reduce costs?

Responses: 3

a). None 2

b) Improve Photo-resist operation 1

(8) Have or will you be doing any work in developing a multi-layer thin film processing technology?

Responses: 9

Yes	No
2	7

(9) Where should government research funds be spent in reducing costs and improving thin film circuit reliability over the next 10-year period?

Responses: 6

a). Develop Thin film dielectric for multilayer applications 1

b) Substrate materials 3

c) Manufacturing Techniques 1

d) At the manufacturers via NOSC San Diego 1

e) Multilayer 1

f) Concentrate on Thick Film 1

Thick Film Circuits

(10) What types of substrate materials do you use, %?

a. Alumina Responses 11

%

75	80	90	99	
1	1	3	6	

b. Beryllic Responses: 8

%

1	3	7	10	25	
4	1	1	1	1	

c. Glass Responses: 2

%

1	10
1	1

d. Porcelanized Steel Responses: 1

%

1
1

(11) What are the current processing limits, typical design, and goals in the following areas?

a. Conductive Layers Responses: 11

	2-3	4-5	6	7	10
max	1	6	2	1	1
Typical	8	1	1		
1987 goal		1	2	3	1

b. Resistors Responses: 9

Value

	<1Ω	10-10M	3 M	10 M	100M
Max.	1		1	5	2
Typical	1	5			
1987 Goal				2	1

TC-PPM Responses: 10

	75-50	100-500	200	25
Max.	6	1	2	
Typical	1	5	4	
1987 Goal	2			4

Tolerance Responses: 9

	+.05 - .1%	+.5-1%	+5%	+10%	+.01%
Max.	2	3		1	
Typical		5	4		
1987 Goal	2	1			1

c. Substrate Area Responses: 10

	1x1½	2x2	2x1	3x3	3x4	4x4	5x5	6x30
Max.	1	2		2	2		1	
Typical	1	3	5	1				
1987 Goal		1		1	1	3	2	1

d. Conductor Lines/Spaces (mils) Responses: 10

	7/7	4/4	5/5	10/10 - 15/15	8/7
Max	3		4		
Typical				9	1
1987 Goal		2	6		

(12) Which conductive materials do you now employ?

Responses: 11

Type	% Use								
	5	10	20	30	40	70	75	90	95
Au		2		1	1	1	2	1	3
Ag Pd	1	3	1	1					
Ag Pt	2	1	1		1				
Cu		1	1		1				
Ag				1					
Au Pt		1							
Other							1		

(13) To reduce material costs are you looking into any non noble metal systems?

Responses: 10

Yes	NO
3	7

a. Cu, Ni 3

(14) What type of resistors do you use in your multilayer thick film circuits?

Responses: 11

Type	% Use							
	0-3	5	10	16	50	80	90	95-100
Chips (thick/thin)		2	2	1	2	1	1	1
Top Dielectric (screened)	4		2					
In Multilayers	4							
On Substrate	1		2		2	1	1	4

(15) Multilayer Substrates - do you 100% DC probe all substrates for shorts/opens?

Responses: 11

Yes	No
5	6

(16) If not, at what point (in complexity) do you find it necessary to 100% DC probe a multilayer thick film substrate?

Responses: 8

Number of Layers

2	3	5	8
1	3	3	1

(17) What is your typical thick film substrate throughput yield?

Responses: 11

(a) 5-25% _____

(b) 25-45% _____

(c) 45-65% 1

(d) 65-85% 6

(e) 85-100% 4

(18) What is your high cost element in thick film processing?

Responses: 9

Element	% of final Substrate costs				
	20	40	50	70	90
a. Resistors	1		1		
b. Printing	1				1
c. Screen Fire				1	

(18) Continued

Element	% of final Substrate Cost				
	20	40	50	70	90
d. Visual inspection			1	1	
e. Au Cond.		1			
F. Prec. Metals	1				

(19) Where are you spending your IR&D funds in the above areas to improve thick film yield (reduce costs/improve reliability)?

Responses: 9

a. Larger area substrates 1

b. Lower cost pastes 1

c. Direct bonded sheet copper 1

d. Compatible multilayer Dielectric & Resistors 2

e. Improving process controls 3

f. Improving screens and design rules 1

g. Automatic testing, inspection 1

h. No IR&D funds 1

(20) Where should the government research funds be spent in reducing costs and improving reliability of thick film circuits in the next 10 years?

Responses: 11

a. Assembly technology 3

b. Non-Noble metal materials 1

c. Improve control and space of improved pastes 1

d. Automated inspection 2

e. Materials 3

(20) continued

f. At manufacturers via NOSC San Diego 1

g. Package sealing 1

RESISTOR TRIMMING

(1) What trimming method do you use for adjusting your resistor valves?

Responses: 12

	Thick Film	Thin Film
Laser	10	6
Abrasive	2	

(2) What process yields can you achieve with the following tolerances?

Responses: 10 Thick Film

% Yield

	9	10	30	60	75	80	90	95	99	100
± 20%					1			1	1	6
± 10%			1				1	2	2	3
± 5 %							2	4		2
± 1 %				1			6			1
± 0.1 %	1	1			1	1				

Thin Film Responses: 10

	% Yield			
	80	90	95	100
± 20%			1	3
± 10%		1	1	2
± 5 %		1	1	2
± 1 %		2		2
± 0.1%	1	1		
0.1 %	1			

(3) Do the trimming techniques used effect reliability?

Responses: 9

Yes 6

No 3

(4) If so, what compensating techniques do you use to prevent this?

Responses: 3

a. Pass hot evaluation 1

b. Retrim or laser trim 1

c. Stabilization bake 1

d. Over design 1

(5) Do you active trim?

Responses: 11

Yes 9

No 2

If yes

(6) What is the cost impact of this operation?

Responses: 8

a. Less costly than maintaining tight component tolerances. 1

b. Generally low 3

c. 2 or 3 per resistor 1

d. None 1

e. Very expensive if not recoverable 1

f. High 1

If no

(7) Do you circumvent active trim by tighter control on other circuit element parameters?

Responses: 9

Yes 2 No 6

Use contact methods to obtain active trim 1

8.0 SUBSTRATE TECHNOLOGY

Hybrids under investigation for this study, as defined in the first section, are assumed to be built on a ceramic substrate.

Responses: 11

(1) What is the primary substrate material used at your facility?

a) Alumina 11

(2) How many different substrate material types do you use?

Responses: 11

1	2	3
2	4	5

(3) Does the substrate material you use meet your processing requirements?

Responses: 11

Yes	NO
10	1

Comments:

1) Want to use ground substrate for multilayer fab on large substrates. 1

(4) What substrate parameters could be improved that would have a direct impact on your processing yields?

Responses: 11

a. Flatness 11
b. Surface Finish 2
c. Binder Material Uniformity 1
d. Size Tolerance 3

(5) What developments would you like to see in the industry to upgrade or replace current substrate materials?

Responses: 8

a. Ceramics seem adequately good now. 3
b. Glazed steel or ceramic to beneficially react with Thick-Film pastes for bond strength. 1
c. Cheaper material. 1
d. Larger size substrate 1
e. Greater thermal conductivity 1
f. Flatter substrates 4
g. Insulated metal substrates 1
h. Flexible materials for direct bonding. 1

(6) What would the advantage be to you in these new substrate materials in reducing hybrid costs and/or improving reliability?

Responses: 7

a. Higher yield. 5
b. Lower costs 3
c. Higher reliability 1
d. Increase interconnection density 1
e. Substrate costs related to producibility 1

(7) What percent of your development funds are dedicated to developing new or improving existing substrate materials?

Responses: 9

0	2	20
7	1	1

9.0 LEAD BONDING

One of the perennial problem areas in the manufacture of discrete semiconductor devices and particularly hybrids is lead attachment to the die and substrate. The problem is aggravated in hybrids because of the varied types of metallization systems encountered on the substrates. In individual hybrid types, it is aggravated by the problem of attachment to die of various manufacture, thickness and surface condition.

Methods of alleviating or eliminating the problem have included beam lead devices, flip chips, tape bonding, single metallic systems, and low tempature bonding techniques. Methods of detecting failures or incipient failures include methods detailed in MIL-STD-883B, Numbers 2010, 2011, and 2017.

(1) Are the following methods of lead attachment satisfactory for complex military hybrids?

Responses: 12

Au wire T/C pulsed TC Yes: 11 No: 1

Comments:

1) Slow
2) Wedge bond is weak
3) Rebond of wedge is difficult

Au Wire Ultrasonic Yes: 10 No: 2

Comments:

1) Slow
2) Wedge bond is weak.
3) Rebond of wedge is difficult

Al Ultrasonic Yes: 9 No: 1

Comments:

1) Slow
2) Wedge bond is weak
3) Rebond of wedge is difficult

Bond Lead Yes: 6 No: 3

Comments:

1) Devices not available
2) Lifting leads to debug is not possible
3) Cannot visually inspect

Flip Chip Yes: 5 No: 3

Comments:

1) Solder bond is not good at high temperature
2) Cannot visually inspect
3) Small selection of devices

Tape Bonding Yes: 8 No: 0

Comments:

1) Depends upon equipment costs, standardization, and selection of devices available.

(2) What other methods or modifications to existing methods must be developed to provide improved reliability levels?

Responses: 6

1) New TIP design to increase bond area of Au wedge bond.
2) Permit pretesting.
3) Need to eliminate wire bonding
4) Use of flexible substrate circuit with direct chip to circuit bonding.
5) Good automatic wire bonding process
6) Standard cleaning method.

(3) Should lead bonding be limited to monometallic systems?

Responses: 12

Yes: 1 If possible: 3 No: 8

(4) Are present visual test requirements adequate? _____strict? _____ loose? _____ Why?

Responses: 11

Adequate: 9 Strict: 1 Loose: 1

Comments:

1) Good bonds often fail visual
2) Bad bonds often pass visual
3) Cannot detect most conditions visually
4) Allows too much to be passed for High Rel. programs

(5) Should high temperature storage precede lead pull tests on sample lots?

Responses: 12

Yes: 7 No: 5

Comments:

1) Limit should be set to meet the predictable degradation
2) Must be done in an inert atmosphere.
3) Not necessary if process is in control.

(6) Should 100% non-destructive pull tests be part of the normal production cycle?

Responses: 12

Yes: 1 No: 10

Comments:

1) Cost is very high (6)
2) Bond strength can be reduced (2)
3) Unnecessary (2)
4) Assures that all bonds are good.
5) Yes, if done automatically

(7) Does present bonding equipment provide the necessary process control for high yields?

Responses: 11

Yes: 7 No: 4

(8) If not, what changes should be made to provide the control necessary?

Responses: 4

1) Tail length must be kept constant
2) More stability in the machine
3) Feedback system to verify bond as it is been applied.
4) Better control equipment and tool design.
5) Needs automatic pull test capability

(9) Automatic lead bonding equipment is used extensively in the semiconductor market. Do you see it taking a significant role in hybrid assemblies in the future?

Responses: 12

Yes: 8 No: 4

Comments:

1) Cost reduction for multichip assembly (6)
2) More repeatablity (less operator error) (3)
3) Lack of Standardization (2)
4) Little use in analog circuits
5) More uniform wire dress.
6) Confusion factor for wire bonders.
7) That is the best alternative

(10) What is the limit on the complexity level of hybrids using Automatic Wire Bonders?

Responses: 9

(a)	1-5 die	1
(b)	5-10 die	1
(c)	10-25	2
(d)	25	4
(e)	No limit	1

(11) If beam lead devices were available for all attached active devices, would you employ beam leads?

Responses: 10

Yes: 2 No: 8

Comments:

1) It is difficult to handle and inspect (5)
2) Dependent upon reliability findings (2)
3) Equipment costs (2)
4) Same problems as wire bonded chips
5) Difficult to bond to thick film metal

(12) Will tape bonding process provide a viable means of fabricating high reliability circuitry:

Responses: 10

Today? Yes: 3 No: 5

Comments:

1) Too costly
2) Not available
3) Already in large scale use
4) Yes, provided good metalurgy used.

In the next 5 years? Yes: 4 Maybe: 1 No: 3

Comments:

1) Immature
2) Industry acceptance
3) Depends upon ability to test and screen devices.

In the next 10 years: Yes: 4 Maybe:1 No: 3

Comments:

1) Need acceptable MIL version at low cost
2) Automatic assembly methods.
3) Depends upon ability to test and screen devices

(13) What do you think will be the greatest deterrent to the successful utilization of the tape technology?

Relative rating 1 through 5.

Responses: 1

	1	2	3	4	5
. Availability of devices	7	2	2	0	0
. Variety of device types	4	3	1	3	0
. Cost of devices	2	1	4	2	2
. Processing equipment	1	2	1	4	2
. Other	1	0	0	0	1

10.0 HYBRID DEVICE ATTACHMENT

The hybrid industry employs numerous methods of device attachment during hybrid assembly. The ideal method would contain the following characteristics:

- Low cost
- Low thermal impedance
- High electrical conductivity
- Compatible with all other materials and processes
- Non-organic
- Infinite rework capability
- Etc.

However, the ideal attachment material is not yet available.

(1) What percentage of your hybrids are assemblied using:

Responses: 11

a) Eutectic Die Attachment

5%	10%	20%	25%	70%
4	3	1	1	2

b) Conductive Epoxy

20-25%	60-65%	75%	80%	95-100%
2	2	2	1	3

c) Non-conductive Exoxy

5%	10%	20%	90%	95%
2	3	1	1	2

d) Teflon

0% (Only one known application)

e) Solder

5%	10%	20%
3	2	1

f) Other

5%	50%
1	1

(2) Which of the above processes are employed in the same hybrid?

Responses: 11

a	b	c	d	e	f
9	11	10	0	3	3

(3) Do your various customers accept the use of a controlled epoxy process for device attachment?

Responses: 11 Yes: 11 No: 1

(4) What problems have you encountered obtaining epoxy approval for use in military hybrids since MIL-M-38510 prohibits its use?

Responses: 7

1) None (4)
2) Obtain waiver prior to receipt of contract (2)
3) Exception MIL-M-38510
4) Outgassing/weight loss
5) Moisture Absorption
6) Qualification history

(5) What problems (yield/cost) do you encounter in using the following attachment methods?

Responses: 10

(a) Eutectic
    1) Double the drop out at die attachment
    2) Repairability
    3) Temperature degradation

(b) Epoxy
    1) None
    2) Outgassing - poor curing
    3) Control

(c) Teflon

(d) Solder.

1) Difficult to remove flux residue
2) Leaching
3) Temperature

(e) Other

(6) Device attachment methods also include items such as beam leads (TC) and flip chips (solder). What material or device developments are required in the next 10 years to perfect device attachment methods?

Responses: 6

1) Hermetically sealed devices
2) Improved metalurgy
3) Beam leads with uniform hardness and bonding characteristics.
4) Better bonding equipment
5) Placement pattern recognition for flip chips
6) Automation
7) Industry committment

11.0 HYBRID ELECTRICAL TESTING

Electrical testing as a means of assuring circuit integrity may occur at several stages in the production of hybrid microcircuits.

Stage 1: Wafer - Prior to scribe and break

Stage 2: Die - Prior to shipment to hybrid manufacturer

Stage 3: Die-After receipt by hybrid manufacturer (Die receiving inspection)

Stage 4: Assembled Hybrid - Prior to lid seal

Stage 5: Sealed Hybrid - Prior to screening

Stage 6: Screened Hybrid - Prior to burn-in

Stage 7: Burned-in Hybrid - Prior to shipment (Final Electrical)

Electrical testing may be performed at various temperatures based on the end product use of the hybrid. Military usage may require $\pm$ 125°C, 25°C and -55°C testing while commercial usage may require only 70°C, 25°C, and 0°C or even just 25°C testing. Other temperatures may be found to be more effective in finding undesirable anomalies.

The type of test performed can have a significant effect on the types of defects found. DC tests can verify electrical continuity while AC tests can find timing, frequence response, or phase shift problems.

TABLE 11-1: DC TESTING CURRENTLY PERFORMED ON YOUR PRODUCT

Insert the appropriate category letter for each type of product you manufacture versus the dc electrical testing the device or die receive during the manufacturing process.

Category	Meaning
H	Space usage - either NASA, military or other; roughly comparable to JAN Level "S" or "A".
M	Military usage - Roughly comparable to JAN Level B
L	Lower reliability military usage such as ground equipment. Roughly comparable to JAN Level C

Note: Indicate guard band testing as 25°C tests with a "G" after the "Category Letter".

Responses: 7

Stage at Which Electrical Test is Performed	DC Test Temperature																							
	-55°C			0°C			Other Low Temp °C -25			25°C			70°C			125°C			Other High Tem °C +105		
	H	M	L	H	M	L	H	M	L	H	M	L	H	M	L	H	M	L	H	M	L
Wafer	1									1	G 5	4				1	1				
Die Pre-ship												1									
Die R&I	1									2	2	G 2				1					
Assembled Hybrid	1	3						1	2	1	G 5	4		1	1		2				1
Sealed Hybrid		4	1			2					4	G 4			2	2	4	1			
Screened Hybrid	1	2	1		1						3	G 2		1		1	2	2			
Burned-in Hybrid	1	6	1			2			1	1	5	G 3			2	1	6	2			1

TABLE 11-2: AC TESTING CURRENTLY PERFORMED ON YOUR PRODUCT

Insert the appropriate category letter for each type of product you manufacture versus the AC electrical testing the device or die receiver during the manufacturing process.

Category	Meaning
H	Space Usage
M	Military Usage
L	Lower Reliability Military Usage
K	Commercial Usage

Note: Indicate guard band testing as 25°C tests with a "G" after the "Category Letter".

Responses: 8

Stage at Which Electrical Test is Performed	AC Test Temperature																					
	-55°C				0°C		Other Low Temp °C -25		25°C				70°C		125°C				Other High Temp °C +105			
	H	M	L	K	L	K	L	K	H	M	L	K	L	K	H	M	L	K	L	K		
Wafer										2	1											
Die Pre-ship		1								1						1						
Die R&I									1	3	2	1										
Assembled Hybrid		1					1		1	5	G 3	1				2			1			
Sealed Hybrid	1	4	1		1	1			1	5	G 3	2	1	1	1	5	2					
Screened Hybrid	1	2	1						2	4	2	2			1	2	2					
Burned-In Hybrid	1	6	2		1	1	1	1	1	6	3	2	1	1	1	5	3	1	1	1		

The requirement (specification imposed) that a test be performed may have little bearing on the effectiveness of a particular test/temperature combination in identifying undesirable performance defects. In your experience, what are the effective combinations of type of test and temperature that will intercept built-in defects (as opposed to maximizing yield)? Insert the end-use category letter in the appropriate boxes you feel should be involved to ensure there are no built-in defects in your product.

TABLE 11-3: DC TESTING THAT YOU FEEL SHOULD BE PERFORMED TO INTERCEPT CIRCUIT DEFECTS

Insert the end-use category letter in the appropriate boxes you feel should be invoked to ensure there are no built-in defects in y our product.

Category	Meaning
H	Space Usage
M	Military Usage
L	Lower Reliability Military Usage
K	Commercial Usage

Responses: 8

Stage at Which Electrical Test is Performed	DC Test Temperature																															
	-55°C					0°C					Other Low Temp °C					25°C					70°C					125°C					Other High Temp °C				
	H	M	L	K		H	M	L	K		H	M	L	K		H	M	L	K		H	M	L	K		H	M	L	K		H	M	L	K	
Wafer																1	5	3	1	G							1	1							
Die Pre-ship		1															3	1								2	1							
Die R&I	1					1	1	1								2	5	3	1	G					2	3	3			G				
Assembled Hybrid	1	3	1				2	2		G						2	6	4	2						1	6	3							
Sealed Hybrid	1	3	1				1	1	1							3	5	4	2		1	1			2	4	1						1	
Screened Hybrid	1	1	1				1	1								2	5	3	1	G					2	2	2							
Burned-In Hybrid	1	3	1				1	1								2	5	3	2	G	1				2	5	2							

TABLE 11-4: AC TESTING THAT YOU FEEL SHOULD BE PERFORMED TO INTERCEPT CIRCUIT DEFECTS

Insert the category letter in the appropriate boxes you feel should be invoked to ensure there are no built-in defects in your product.

Category	Meaning
H	Space Usage
M	Military Usage
L	Lower Reliability Military Usage
K	Commercial Usage

Responses: 7

	AC Test Temperature																				
Stage at Which Electrical Test is Performed	-55°C				0°C				Other Low Temp °C	25°C				70°C		125°C				Other High Temp °C
	H	M	L	K	HM	L	K			H	M	L	K	HMLK		HM	L	K		
Wafer											1	1					1	1		
Die Pre-ship											2	1					1	1		
Die R&I		1								1	2	2	1		1	1	3	2		
Assembled Hybrid		2	1		1	1	1	1		2	6	4	2		1	1	5	3		
Sealed Hybrid	1	4	1		1	1	2	1		2	4	2	1	1	2	2	4	2		
Screened Hybrid	1				1	1	1			2	5	3	2		1	2	2	2		
Burned-In Hybrid	1	4	1		1	1	2	1		2	5	4	3		1	2	2	6	2	

TABLE 11-5: PERFORMANCE OF 100% BURN-IN SCREEN

One hundred percent burn-in and high temperature stress have been touted as useful indicators of device integrity by identifying early failures in the log-normal failure distribution.

Insert the appropriate code indicating the type of thermal stress used on your hybrid product. Indicate the stages (1) where you currently perform (or have performed for you) burn-in or other types of thermal stress, (2) where you plan to perform the stress in the future, and (3) where you think the stress <u>should</u> be performed in the interests of adequate reliability and low cost.

Code	Meaning
HTOL-DC	High nemperature Operating Life (Burn-in) with DC Bias
HTOL-AC	High Temperature Operating Life (Burn-in) with AC Bias
HTRB	High Temperature Reverse Bias
SB	Stabilization Bake
HTS	High Temperature Storage

Also indicate Duration of Test and Test Temperatures
Example: HTOL-AC (160 hrs @ 125°)

Responses: 8

	Type of 100% Burn-In or Other Type of Thermal Stress		
Stress at Which Thermal Stress Test is Performed	Currently Used	Plan to Use	<u>Should</u> be Used
Wafer			
Die Pre-ship			
Die R&I			
Assembled Hybrid	SB (2M @ 125°C) 150°C 1 1 HTOL-DC 72 hrs. 125°C 3	SB (2M @ 125°C) 1	SB (2M @ 125°C) 1 HTOL-AC 160 hrs. 2
Sealed Hybrid			
Screened Hybrid	HTOL-DC 160 hrs. @ 125°C 8	HTOL-DC 160 hrs	HTOL-AC 160 hrs. @ 125°C 3

Electrical testing costs money in two ways:

Direct Test Costs:	Performing the test takes time and costs money
Indirect Test Costs:	A yield loss may occur when the test is performed causing the remaining good parts to cost more

This means that a tradeoff exists between spending a lot of test time (money) early in the hybrid fabrication process to test and remove low-cost defective devices or spending a little test time late in the fabrication process to test and remove high cost-defective devices.

Please indicate on the charts the normalized cost of performing DC tests at three temperatures and AC tests at 25°C. Also indicate the normalized costs due to yield loss at each stage of fabrication.

TABLE 11-6: TEST COSTS vs. YIELD COSTS FOR SMALL SCALE HYBRIDS*

Assume Electrical Test consists of : DC tests at 3 temperatures (example:-55°C, 25°C, 125°C)

AC tests at 25°C

Responses: 2

Stage at Which Electrical Test is performed	Normalized Cost: Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level	Normalized Cost: Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level
Wafer	1 (1)	
Die Pre-ship	1 (1)	
Die R&I	1 (1)	
Assembled Hybrid		
Sealed Hybrid	4 (1)	6 (1)
Screened Hybrid	4 (1)	2 (1)
Burned-In Hybrid	8 (1)	2 (1)

*Less than 100 Equivalent gate functions.

TABLE 11-7: TEST COST vs. YIELD COSTS FOR LARGE SCALE HYBRIDS*

Assume Electrical Test consists of:
- DC test at 3 temperatures (example: -55°C, 25°C, 125°C)
- AC tests at 25°C

Responses: 1

Stage at Which Electrical Test is performed	Normalized Cost: Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level	Normalized Cost: Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level
Wafer		
Die Pre-ship		
Die R&I		
Assembled Hybrid		
Sealed Hybrid	6 (1)	7.25 (1)
Screened Hybrid	3 (1)	3.4 (1)
Burned-In Hybrid	1.5 (1)	2.2 (1)

*100-1000 equivalent gate functions

TABLE 11-8: TESTS COSTS vs. YIELD COSTS FOR VERY LARGE SCALE HYBRIDS*

Assume Electrical Test consists of:
- DC tests at 3 temperature (example: -55°C, 25°C, 125°C)
- AC tests at 25°C

Responses: 1

	Normalized Cost	
Stage at Which Electrical Test is performed	Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level	Percent of Final Sales Price that would be caused by the direct cost of 100% electrical testing at each level
Wafer		
Die Pre-ship		
Die R&I		
Assembled Hybrid		
Sealed Hybrid	7.2 (1)	8.6 (1)
Screened Hybrid	3.6 (1)	3.8 (1)
Burned-In Hybrid	1.8 (1)	2.0 (1)

*Greater than 1000 equivalent gate functions.

Many of the screens and electrical tests called out in cusomer specifications or MIL specifications no longer correctly address the problems which they were originally designed to solve. Elimination of certain of these requirements would possibly save money withou jeopardizing reliability. Please indicate the appropriate category for each of the tests you now may have to perform on hybrid microcircuits.

TABLE 11-9: SUGGESTED CHANGES TO SCREENS AND TESTS

Screen or Test MIL-STD-883B Method 5008	Category I Could Eliminate With No Impact on Reliability	Category 2 Could Eliminate In Some Cases But Would Have Some Impact on Reliability	Category 3 Necessary for Adequate Reliability
DC Electricals	1	1	4
Pre-Seal Burn-In	2		1
Internal Visual		1	4
Stab. Bake	1	2	2
Temp Cycle	1	2	1
Mechanical Shock	4		1
Centrifuge	1	2	1
Visual Inspection	1	1	3
Interim Electrical Parameters		1	1
Subgroups			
1	1	1	
2		1	
3		1	
4	1	1	
5		1	
6		1	
7		1	
8		1	
9		1	
Burn-In-Powered	1	2	3
- Unpowered	1	2	

TABLE 11-9: (Continued)

	Category I	Category 2	Category 3
Seal			1
Fine		2	2
Gross		1	2
Final Electrical Parameters:		1	
Subgroups 1			1
2		1	
3		1	
4			11
5		1	
6		1	
7			1
8		1	
9		1	
External Visual	1	1	1
Other Tests Required		1	

Please describe any additional changes or actions you feel must be enacted to reduct the cost of testing hybrid microcircuits in the 1980's

Final Electrical Test - Eliminate Room Temperature Tests

Very Large Scale Hybrids (VLSH) are becoming very common but test technology has not kept pace. As a result there is a threat that testing costs will drive the price of VLSHs up to prohibitive levels.

Responses: 6

Please list in descending order the highest cost factors you encounter in testing of VLSHs.

Examples:

1	2	3	4	5
	2	2		
2	1		2	
	1	1		1
3			1	1
				3
				1
1				
	2			
1				1

* One time set-up costs for performance boards for automatic test equipment.
* Software development for automatic test equipment.
* Accidental electrical abuse.
* Lengthy test times stretching into hours per part.
* Time required for large packages to stablize at the desired test temperature.
* Others that you see in your operation.
* Data Recording
* Test Specs
* Test Fixturing

12.0 GENERAL COMMENTS

The brief survey questionnaire you have just completed was not intended to obtain answers to any problem areas in the hybrid industry. The intent was to identify cost/reliability problem areas that are affecting the successful application of hybrids in military avionic systems. If there are any areas of concern that you have and we have not addressed in this questionnaire concerning hybrid cost/reliability problems, please take this opportunity to do so at this time. Thank you for your assistance.

Responses: 2

Should have covered hermetic carrier technology 1

Difficult to generalize in answering 1